HIROKI ENDO

he2305@columbia.edu | (646) 281-1401 | endohi.net | linkedin.com/in/endohiroki

EDUCATION

Columbia University, Columbia Engineering **New York, NY**
M.S. in Electrical Engineering | Cumulative GPA: 4.0 *Aug 2024 - Jan 2026*

- Courses: Advanced Logic Design; Digital VLSI Circuits; HW/SW Formal Verification; VLSI Design Lab; Embedded System
- Honor: Electrical Engineering Tesla Scholar 2024

Waseda University, School of Advanced Science and Engineering **Tokyo, JP**
B.Eng. in Physics | Cumulative GPA: 3.9 / 4.0 [US equivalent: 4.0 / 4.0] *Sep 2020 - Jul 2024*

- Minors: Electrical Engineering; Computer Science and Communication Engineering
- Honors: Dean's Honor in Academic Performance 2023 & 2022; Otsuka Toshimi Scholarship 2021

PROFESSIONAL EXPERIENCES

Yamashita Sekkei, Inc. **Tokyo, JP**
Electrical Engineer Intern × Renesas Electronics Corporation *Oct 2023 - Apr 2024*

- Managed and coordinated interns in assisting Power Management IC (PMIC)'s Register Transfer Level (RTL) to GDSII VLSI design flow intro, resulted in reduction of 5 weeks in departmental training time while supporting team collaboration.
- Implemented fundamental digital designs utilizing Verilog reaching functional accuracy through rigorous systems level and RTL simulation and verification with PMIC considerations, led to smoother hand-off to physical design teams.
- Designed and tested DC-DC Buck converter circuits for microcontroller units that contributed to household embedded systems with 35% lower peak power consumption, yielded more efficient system performance.

VeriSilicon Microelectronics Co., Ltd. **Shanghai, CN**
Back-end Engineer Intern, Design Implementation Department *Jul 2023 - Sep 2023*

- Optimized timing closure in Clock Tree Synthesis (CTS) to achieve target clock latency and global skew by analyzing insertion delay and skew during Place-and-Route (PnR) stage, resulted in 58% clock skew reduction and increased product reliability.
- Addressed Clock Transition and Maximum Capacitance issues during PnR stage and resolved violations earlier than standard ECO stage fixes using Synopsys ICC2, improved signal integrity and saved potential rework and tape-out delays.

SemiDrive Technology Ltd. **Shanghai, CN**
Product Engineer Intern, SoC Architecture Department *Mar 2023 - Apr 2023*

- Collaborated in system architecture design of automotive-grade System-on-Chip (SoC), including physical, power, and thermal verification in post-layout stage, provided seamless functionality across various corners and enhanced product reliability.
- Validated prototype SoC by analyzing input/output interface signal and internal registry across extreme operating conditions along with criteria of reality-simulation comparisons, identified faults in early-phase and intercepted potential recalls.

PROJECTS

(Back-end Leader) RISC-V Tape-out - Sponsored by Apple Inc. [URL: ee.columbia.edu/~kinget/vlsidesignlab] **Jan 2025 - Now**

- Designing and taping-out 2mm^2 32-bit SoC based on OpenHW's FPU core and PULP's peripheral IP in TSMC-65nm node, integrating I^{2}C,SPI,UART interfaces, GPIOs, AHB-APB buses and bridge, SRAM, on-chip timer, FSM, and DFT scan chain.
- Expecting full front and back-end flow with architecture design, RTL design, testbench verification, PnR, STA, post-APR verification, layout verification, emulation, GDSII generation, signoff, and anticipating extensive post-silicon validation.

Dual-clock 64-tap Digital FIR Filter Design and Formal Verification [URL: endohi.net/fir-filter] **Aug 2024 - Jan 2025**

- Developed RTL for ALU, CMEM, Shift Register, fixed-to-floating-point converter, and FSM modules from MATLAB model.
- Utilized Synopsys for RTL to gate-level synthesis, STA and power analysis, ensuring constraint compliance and reliability.
- Achieved 150kS/s 16-bit fixed/floating-point samples for FIFO input/output rate, at 100MHz frequency and 4.39pJ/s efficiency.
- Conducted assertion-cover-assumption-based formal verification of ALU and floating-point modules using JasperGold, achieving full stimuli coverage and 90+% formal coverage and ensuring functional correctness with IBM-130nm library.

8-bit Microprocessor Core Design [URL: endohi.net/vlsi-design] **Aug 2024 - Dec 2024**

- Led full logic-to-GDSII flow of a microprocessor in TSMC-65nm node, including ALU, PLA, SRAM, FSM, and multiplexer.
- Simulated clock cycle timing with Spectre and Ultrasim and implemented dataflow functional units with integrated memory.
- Delivered compact DRC & LVS clean layout and optimized device sizing to balance power-performance-area, resulting in 118µm × 136µm area and 28.61mW power at typical corner conditions while executing instruction set reliably at 250 MHz.

TECHNICAL SKILLS

Programming	System Verilog (HDL), Verilog (HDL), Python, C, C++, Java, C#, TCL, Perl, Linux, MATLAB, TensorFlow
Hardwares	TSMC-65nm Node Tech, Embedded Systems Design, Oscilloscope, Network Analyzer, SMT / TH Soldering
Softwares	Cadence *Spectre* & *Virtuoso* & *Innovus* & *JasperGold*, Synopsys *ICC2* & *Design Compiler* & *PrimeTime*, Mentor *Calibre*, ANSYS *Maxwell* & *HFSS*, LTspice, Altium Designer, CUDA, Fusion 360
Languages	English, Japanese, Mandarin